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Attorney Docket No.: P12564

Amendments to the Claims

1. (currently amended) A system for simulating machine instructions on a host machine comprising:
  - a monitor that translates the machine instructions into translated code, the monitor modifying original values in a descriptor table to prevent the translated code from being accessed, thereby preventing the translated code from being modified;
  - a virtual machine that executes the translated code stored in memory; and
  - a kernel that detects exceptions occurring in the virtual machine and transfers control between the virtual machine and the monitor according to a type of the exceptions,wherein an operating system executing on the host machine also supports a full platform simulator that includes device models, the simulator to execute the translated code that represents simulated operating system code to be executed on the virtual machine.
2. (canceled)
3. (currently amended) The system of claim 1 wherein the translated code and the original machine instructions access the memory using ~~[[the]]~~ a same set of addresses.
4. (original) The system of claim 1 wherein the monitor further includes an auxiliary simulator that executes the machine instructions.
5. (original) The system of claim 1 wherein the monitor replaces one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine.
6. (canceled)

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7. (currently amended) The system of claim [[6]] 1 wherein the monitor modifies the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code.
8. (currently amended) The system of claim [[6]] 1 wherein the monitor modifies the descriptor table to replace a segment with a substitute segment, which, when accessed, causes an exception to be generated.
9. (currently amended) A method of simulating machine instructions on a host machine comprising:
- translating the machine instructions into translated code;
  - storing the translated code in memory;
  - executing the translated code;
  - preventing the translated code from being modified;
  - detecting exceptions in the execution of the translated code; and
  - transferring control to an appropriate simulation module on the host machine according to a type of the exceptions,
- wherein an operating system executing on the host machine also supports a full platform simulator that includes simulation modules and device models, the simulator to execute the translated code that represents simulated operating system code to be executed on a virtual machine.
10. (original) The method of claim 9 further comprising simulating a device.
11. (previously amended) The method of claim 9 further comprising accessing memory by the translated code using a same set of addresses as a set of addresses used by the original machine instructions.

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12. (original) The method of claim 9 further comprising replacing one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine.

13. (original) The method of claim 9 further comprising modifying a descriptor table to prevent the translated code from being modified, the descriptor table including attributes of a segment of the memory.

14. (previously amended) The method of claim 13 further comprising modifying the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code.

15. (original) The method of claim 13 further comprising modifying the descriptor table to replace the segment with a substitute segment, which, when accessed, causes an exception to be generated.

16. (currently amended) A computer program product residing on a machine readable medium comprising instructions for causing a host machine to:

- translate a set of machine instructions into translated code;
- store the translated code in memory;
- execute the translated code;
- prevent the translated code from being modified;
- detect exceptions in the execution of the translated code; and
- transfer control to an appropriate simulation module on the host machine according to a type of the exceptions,

wherein an operating system executing on the host machine also supports a full platform simulator that includes device models, the simulator to execute the translated code that represents simulated operating system code to be executed on a virtual machine.

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17. (previously amended) The computer program product of claim 16 further comprising instructions for causing the host machine to simulate a device.

18. (previously amended) The computer program product of claim 16 further comprising instructions for causing the host machine to access memory by the translated code using a same set of addresses as a set of addresses used by the original machine instructions.

19. (previously amended) The computer program product of claim 16 further comprising instructions for causing the host machine to replace one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine.

20. (previously amended) The computer program product of claim 16 further comprising instructions for causing the host machine to modify a descriptor table to prevent the translated code from being modified, the descriptor table including attributes of a segment of the memory.

21. (previously amended) The computer program product of claim 20 further comprising instructions for causing the host machine to modify the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code.

22. (previously amended) The computer program product of claim 20 further comprising instructions for causing the host machine to modify the descriptor table to replace a segment with a substitute segment, which, when accessed, causes an exception to be generated.

23. (newly added) A system for simulating an instruction set architecture on a platform comprising:

a virtual machine monitor to translate the machine instructions of a target processor into translated code, the target processor to run in a virtual machine on the platform, the virtual

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machine monitor to modify original values in a descriptor table to prevent the translated code from being accessed, thereby preventing the translated code from being modified;

the virtual machine to execute the translated code stored in memory; and

a virtual machine kernel to detect exceptions occurring in the virtual machine and to transfers control between the virtual machine and the virtual machine monitor according to a type of the exceptions,

wherein an operating system executing on a host machine on the platform supports a full platform simulator that includes device models, the simulator to execute the translated code that represents simulated operating system code to be executed on the virtual machine, thereby allowing the target processor to be simulated without disturbing the operating system running on the host machine.

24. (newly added) The system of claim 23, wherein the translated code and the original machine instructions access the memory using a same set of addresses.

25. (newly added) The system of claim 23, wherein the virtual machine monitor further includes an auxiliary simulator that executes the machine instructions.

26. (newly added) The system of claim 23 wherein the virtual machine monitor is to replace one of the machine instructions with a capsule if the machine instruction accesses a system state of a central processing unit of the host machine, the capsule being one of a simple capsule and a complex capsule, and wherein simple capsule is executed by the virtual machine and a complex capsule is executed by the virtual machine monitor.

27. (newly added) The system of claim 23, wherein the virtual machine monitor modifies the descriptor table to remove a portion of a segment that overlaps with the memory storing the translated code.

28. (newly added) The system of claim 23, wherein the virtual machine monitor modifies the descriptor table to replace a segment with a substitute segment, which, when accessed, causes an exception to be generated.